Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

claims 1-10 (cancelled)

11. (new) A semiconductor structure, comprising:

a substrate;

a memory element comprising a gate including a gate oxide layer on the substrate, a floating gate, and a control electrode capacitively coupled to the floating gate, wherein a signal for controlling the memory element is applicable to the control electrode, wherein the floating gate comprises a first floating gate portion and a second floating gate portion connected with each other, the first floating gate portion being formed on the gate oxide layer, the second floating gate portion being laterally and vertically shifted from the first floating gate portion, and wherein the control electrode and the second floating gate portion are disposed opposite to each other with an oxide layer therebetween; and

a plurality of metallization layers formed in a portion above the memory element and fully covering the floating gate, wherein at least one of the metallization layers is used as a shield layer for the floating gate,

wherein in case the distance of the control electrode to the surface of the substrate is smaller than the distance of the second floating gate portion to the surface of the substrate, the

shield is formed by connecting a metallization layer farthest from the second floating gate portion to the substrate, and

wherein in case the distance of the second floating gate portion to the surface of the substrate is lower than the distance of the control electrode to the surface of the substrate, the shield is formed by connecting a metallization layer closest to the control electrode to the substrate.

12. (new) The semiconductor structure according to claim 11, wherein the memory element is formed at least partly in the substrate, wherein a potential is applicable to the substrate and/or to the well, and wherein, when the memory element is formed at least partly in the well in the substrate, the metallization layer forming the shield is connected to the well.

13. (new) The semiconductor structure according to claim 12, wherein the substrate and/or the well shields the floating gate.

14. (new) A semiconductor structure comprising:

a substrate;

a first portion formed on the substrate comprising a memory element including a floating gate and a control electrode capacitively coupled to the floating gate;

a second portion formed on the first portion comprising a control terminal for controlling the control electrode, and a shield for the floating gate:

wherein the shield is connected to the substrate; and

wherein the control terminal is operably connected to the control electrode by way of a connection that extends through the second portion of the substrate.

15. (new) The semiconductor structure of claim 14, wherein the second portion includes a plurality of metallization layers; and

further wherein at least one of the metallization layers is used as the shield for the floating gate.

16. (new) The semiconductor structure of claim 15, wherein the control electrode is arranged between the floating gate and the plurality of metallization layers; and

further wherein a metallization layer of the plurality of metallization layers that is closest to the control electrode is used as the shield for the floating gate.

17. (new) The semiconductor structure of claim 15, wherein the floating gate is arranged between the control electrode and the plurality of metallization layers; and

further wherein a metallization layer of the plurality of metallization layers that is farthest from the control electrode is connected to be used as the shield for the floating gate.

18. (new) The semiconductor structure of claim 15, wherein more than one of the metallization layers are used for the shield, and

further wherein each of the more than one metallization layers that are operably connected to each other and at least one of the more than one metallization layers is connected to the substrate.

19. (new) The semiconductor structure of claim 14, wherein the shield is operably coupled to the control terminal.

20. (new) The semiconductor structure of claim 14, wherein the floating gate comprises a first floating gate portion and a second floating gate portion connected with each other, the first floating gate portion being formed on a gate oxide layer, the second floating gate portion being laterally and vertically shifted from the first floating gate portion, and wherein the control electrode and the second floating gate portion are disposed opposite to each other with an oxide layer therebetween.